

METHOD AND APPARATUS FOR DESIGNING  
SEMICONDUCTOR INTEGRATED CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

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This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-303495, filed on August 27, 2003, the entire contents of which are incorporated herein by reference.

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BACKGROUND OF THE INVENTION

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The present invention relates to an apparatus and a method for efficiently designing a semiconductor integrated circuit.

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To produce a semiconductor integrated circuit (LSI), a floor plan is designed based on a netlist obtained through logic synthesizing. Cells are arranged and routed in accordance with the floor plan to layout the circuit in detail. The circuit undergoes simulation to determine whether the layout of the circuit guarantees signal integrity (SI) and power integrity (PI).

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The determination of whether the SI or the PI may be guaranteed is performed by determining whether or not an IR drop value (voltage drop value) exceeds a maximum value or by determining whether or not the value of the current flowing through an input/output buffer (hereafter referred to as IO buffer) exceeds a current capacity value. When the SI and PI cannot be guaranteed, the layout of the circuit must be redesigned.

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The redesigning increases the design time and raises the design cost. It is thus important that redesigning be decreased.

One reason causing the IR drop value to exceed a maximum value (hereafter referred to as maximum IR drop value) or causing the value of the current flowing through the IO buffer to exceed the current capacity value (hereafter referred to as current capacity) is in that the quantity and locations (provisional quantity and provisional locations) of power supply pads determined through initial designing prior to the detailed routing of the circuit is inappropriate. Thus, in the prior art, the provisional quantity and locations of the power supply pads cannot be accurately determined.

In one prior art example, the provisional quantity and locations of the power supply pads are determined as described below.

(1) Rules are established based on past experience to obtain the quantity of power supply pads required to reduce simultaneous switching noise in an output buffer. The quantity of power supply pads is determined in accordance with the rules.

(2) A clock buffer or the like is adjoined each power supply pad for the noise decrease.

In the prior art, the determination of the provisional quantity and provisional locations of the power supply pads is based on past experience mainly from the viewpoint of countering noise.

Japanese Laid-Out Patent Publication Nos. 11-297840 and 10-294380 describe processes for estimating chip size (more specifically, core size) before laying out the circuitry. In the process described in Japanese Laid-Out Patent Publication No. 11-297840, when predicting the wire length of a core section, factors of a netlist that affect the value of the wire length is not taken into consideration. In the process described in Japanese Laid-Out Patent Publication No. 10-294380, the wire region required around a circuit block is

determined from the arrangement of the circuit block.

#### SUMMARY OF THE INVENTION

5        One aspect of the present invention is a method for provisionally determining quantity and positions of a plurality of power supply pads when designing a semiconductor integrated circuit including a core section provided with a plurality of nodes and the plurality of power supply pads,  
10        with each power supply pad being connected to the core section via an IO buffer. Each IO buffer has a predetermined current capacity. The method includes performing a power supply network analysis of the core section based on power consumption information of the core section and power supply  
15        wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes. The method further includes calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes, calculating current values of  
20        the power supply pads from the current values between the nodes, determining whether the current value of each of the power supply pads exceeds the current capacity of the associated IO buffer, and eliminating or adding at least one power supply pad in accordance with the result of the  
25        determination.

      Another aspect of the present invention is a method for provisionally determining quantity and positions of a plurality of power supply pads before detailed design of a semiconductor integrated circuit. The semiconductor integrated  
30        circuit includes a core section provided with a plurality of nodes and a plurality of power supply pads. The method includes initially defining all of the pads as power supply pads at which the potential is the same, and performing a

power supply network analysis of the core section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes.

5 The method further includes calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes, calculating current values of the power supply pads from the current values between the nodes, determining whether there is a power supply pad for  
10 which current value is less than or equal to a predetermined current capacity, and adding a new power supply pad near a power supply pad for which current value exceeds the predetermined current capacity, and assigning a power supply pad as another type of pad when the current value of that  
15 power supply pad is less than or equal to the predetermined current capacity.

A further aspect of the present invention is a method for estimating the size of a core section of a semiconductor integrated circuit. The core section includes a plurality of  
20 nets, each including a plurality of wires. The method includes calculating the total net length of the wires of the nets and usable channel length of the core section by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit. The total net  
25 length is the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction, and the usable channel length is the sum of a channel length in the first direction  
30 and a channel length in the second direction. The method further includes calculating the total length of the first wires, calculating the total length of the second wires, and determining the size of the core section that satisfies

conditions of the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction.

A further aspect of the present invention is a method for estimating the size of a core section in a semiconductor integrated circuit provided with a plurality of circuit blocks and the core section, which includes a plurality of repeater cells arranged between the circuit blocks. The method includes calculating the total area of the circuit blocks, calculating the area of a wire region extending around each circuit block to receive wires in order to calculate the total area of the wire regions of the circuit blocks, calculating the total area of the repeater cells, and calculating the size of the core section by totaling the total area of the circuit blocks, the total area of the wire regions, and the total area of the repeater cells.

A further aspect of the present invention is a method for estimating provisional wire capacitance in a semiconductor integrated circuit including a plurality of nets, each having a plurality of wires. The method includes calculating an average path length for nets having the same fan-out by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit, calculating an average net length of the nets having the same fan-out based on the average path length calculated for nets having the same fan-out, and estimating the provisional wire capacity for nets having the same fan-out based on the average net length and the capacity per unit length of the associated wires.

A further aspect of the present invention is a method for estimating the size of a chip for a semiconductor integrated

circuit provided with at least one core section and a plurality of power supply pads. The core section includes a plurality of nets, each having a plurality of wires, and each of the power supply pads being connected to the core section via an IO buffer having a predetermined current capacity. The method includes calculating the total net length of the wires of the nets and the usable channel length of the core section by referring to circuit information and a layout parameter that are used to design the semiconductor integrated circuit.

The total net length is the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction. The usable channel length is the sum of a channel length in the first direction and a channel length in the second direction. The method further includes determining the size of the core section that satisfies conditions of the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction. Additionally, the method includes performing a power supply network analysis of the core section based on power consumption information of the core section and power supply wire resistance information, which includes resistances between the nodes, to calculate voltage values of the nodes, calculating current values between the nodes from the voltage values of the nodes and the resistances between the nodes, calculating current values of the power supply pads from the current values between the nodes, determining whether there is a power supply pad for which current value exceeds the predetermined current capacity, eliminating or adding a power supply pad in

accordance with the determination result and determining the quantity and locations of the power supply pads to calculate the area of an IO region in accordance with the determined quantity, and totaling the size of the core section and the  
5 area of the IO region.

A further aspect of the present invention is an apparatus for designing a semiconductor integrated circuit including a core section provided with a plurality of nodes and a plurality of power supply pads. The core section has a  
10 plurality of nets, each including a plurality of wires. Each power supply pad is connected to the core section via an IO buffer. Each IO buffer has a current capacity. The apparatus includes a storage device which stores power consumption information of the core section and power supply wire  
15 resistance information, including resistances between the nodes. A data processor is in communication with the storage device. The data processor performs a power supply network analysis of the core section by referring to the power consumption information and the power supply wire resistance  
20 information to calculate voltage values of the nodes, calculates current values between the nodes from the voltage values of the nodes and the resistances between the nodes, calculates current values of the power supply pads from the current values between the nodes, determines whether the  
25 current value of each of the power supply pads exceeds the current capacity of the associated IO buffer, and eliminates or adding a power supply pad in accordance with the result of the determination to determine the quantity and locations of the power supply pads.

30 A further aspect of the present invention is an apparatus for designing a semiconductor integrated circuit having a core section provided with a plurality of nets, each including a plurality of wires. The apparatus includes a storage device

which stores circuit information and a layout parameter that are used to design the semiconductor integrated circuit. A data processor is in communication with the storage device. The data processor calculates the total net length of the  
5 wires of the nets and the usable channel length of the core section by referring to the circuit information and the layout parameter. The total net length is the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires  
10 extending in a second direction perpendicular to the first direction. The usable channel length is the sum of a channel length in the first direction and a channel length in the second direction. The data processor further determines the size of the core section that satisfies conditions including  
15 the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction.

20 A further aspect of the present invention is an apparatus for designing a semiconductor integrated circuit provided with a core section and a plurality of power supply pads. The core section includes a plurality of nodes and a plurality of nets, each net having a plurality of wires. Each of the power supply  
25 pads is connected to the core section via an IO buffer having a predetermined current capacity. The apparatus includes a storage device which stores power consumption information of the core section, power supply wire resistance information, which includes resistances between the nodes, and circuit  
30 information and a layout parameter that are used to design the semiconductor integrated circuit. A data processor is in communication with the storage device. The data processor calculates the total net length of the wires of the nets and



the usable channel length of the core section by referring to the circuit information and the layout parameter. The total net length is the sum of the lengths of a plurality of first wires extending in a predetermined first direction and the lengths of a plurality of second wires extending in a second direction perpendicular to the first direction, and the usable channel length is the sum of a channel length in the first direction and a channel length in the second direction. The data processor further determines the size of the core section that satisfies conditions of the total net length being less than or equal to the usable channel length, the total length of the first wires being less than or equal to the channel length in the first direction, and the total length of the second wires being less than or equal to the channel length in the second direction. Additionally, the data processor performs a power supply network analysis of the core section by referring to the determined size of the core section, the power consumption information, and the power supply wire resistance information to calculate voltage values of the nodes. The data processor further calculates current values between the nodes from the voltage values of the nodes and the resistances between the nodes, calculates current values of the power supply pads from the current values between the nodes, determines whether there is a power supply pad for which current value exceeds the current capacity of the associated IO buffer, and eliminates or adds a power supply pad in accordance with the result of the determination to determine the quantity and locations of the power supply pads.

In the present invention, conditions of IR drop value and IO buffer current capacity that guarantee SI and PI can be satisfied when the circuit is laid out for the first time. As a result, redesigning of the layout of the circuit and a major correction, such as reselecting the LSI package or changing

the chip size will not be necessary. In the present invention, when estimating the wire length of a core section, factors of a netlist that affect the value of the wire length is taken into consideration. Thus, the core size can be accurately  
5 estimated. Further, in the present invention, a circuit block and the wire region required around the circuit block are determined. Thus, even if there are many circuit blocks, it is easy to accurately estimate the core size.

Other aspects and advantages of the present invention  
10 will become apparent from the following description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

#### BRIEF DESCRIPTION OF THE DRAWINGS

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The invention, together with objects and advantages thereof, may best be understood by reference to the following description of the presently preferred embodiments together with the accompanying drawings in which:

20 Fig. 1 is a flowchart illustrating a process for estimating chip size according to a first embodiment of the present invention;

Fig. 2 is a schematic diagram of a designing apparatus according to the first embodiment of the present invention;

25 Fig. 3 is a flowchart illustrating a process for estimating the quantity and locations of power supply pads according to the first embodiment of the present invention;

Fig. 4 is a flowchart illustrating the flowchart of Fig. 3 in detail;

30 Fig. 5A is a schematic diagram of a chip prior to elimination of power supply pads;

Fig. 5B is a schematic diagram of a chip subsequent to elimination of power supply pads;

Fig. 6 is a model circuit diagram used to calculate the current amount flowing through the power supply pads;

Fig. 7 is a diagram illustrating an elimination process;

Fig. 8 is a diagram illustrating the bias (or  
5 distribution) of the power supply wire density;

Fig. 9 is a diagram illustrating a layout example of a high-speed operation module;

Fig. 10 is a diagram illustrating the bias (or  
10 distribution) of the current amount flowing through the power supply pads;

Fig. 11 is a flowchart illustrating a process for estimating core size according to the first embodiment of the present invention;

Fig. 12 is a flowchart illustrating a process for  
15 estimating core size according to a second embodiment of the present invention;

Fig. 13 is a diagram illustrating a layout block;

Fig. 14 is a diagram illustrating the quantity of wires required for terminals;

Fig. 15 is a diagram illustrating wires that pass by the  
20 layout block; and

Fig. 16 is a flowchart illustrating a procedure for estimating the quantity of wires that must detour a circuit  
block.

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#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A designing method and designing apparatus for a semiconductor integrated circuit (LSI) according to a first  
30 embodiment of the present invention will now be discussed. In the designing method, the first embodiment relates to initial designing that is performed before designing the layout of a semiconductor integrated circuit.

Fig. 1 is a flowchart illustrating a process for estimating chip size during initial designing. The process is executed by a central processing unit (CPU) 22 of a designing apparatus 21, which is shown in Fig. 2. The CPU 22 functions  
5 to calculate power consumption, calculate power supply wire density, estimate core size, determine quantity and locations of power supply pads, and determine chip size.

In step S1, the CPU 22 calculates the power consumption of a core section referring to a netlist file F1 obtained  
10 through logic synthesizing, a wire capacitance file F2, and a transistor (Tr) activation rate file F3 to generate a power consumption file F4.

In step S2, the CPU 22 calculates the power supply wire density that does not cause the IR drop value to exceed the  
15 maximum IR drop value (i.e., satisfy the IR drop conditions) in the core section to generate a power supply wire density file F5. The power supply wire density is the area of the power supply wire per unit area of the core section or the volume of the power supply wire per unit volume of the core  
20 section.

In step S3, the CPU 22 estimates the core size that ensures the signal wire channel region that is to be formed on the core section based on the power supply wire density file F5 generated in step S2, a circuit information file F6  
25 generated from the netlist file F1, and a layout parameter file F7. Step S3 will be described in detail later.

Prior to step S4, the CPU 22 generates a power supply wire resistance file F8 from the netlist file F1.

In step S4, the CPU 22 determines the quantity and  
30 locations (provisional quantity and provisional locations) of the power supply pads based on the power consumption file F4 and the power supply wire resistance file F8. The arrangement of some power supply pads may be restricted to certain

locations. For power supply pads subject to such restrictions, the CPU 22 refers to a pad restriction information file F9, which records restriction information, to roughly, or provisionally, estimate the quantity and locations of the power supply pads. The provisional quantity and provisional locations of the power supply pads obtained in step S4 are used as initial values that are used to design the layout of the semiconductor integrated circuit. Step S4 will be described in detail later.

In step S5, the CPU 22 checks whether the core size estimated in step S3 enables the routing of the provisional quantity of power supply pads at the provisional locations, which have been determined in step S4. When routing is possible, the area required for routing the power supply pads (more specifically, the area of an IO region including an IO buffer) and the area required in subsequent processes are added to the core size estimated in step S3 to estimate the chip size. When routing is not possible, the chip size is estimated after enlarging the core size obtained in step S3 to a size that enables routing of the power supply pads obtained in step S4.

Fig. 2 is a schematic diagram of a designing apparatus in the present embodiment. The designing apparatus 21 has the same configuration as a typical computer aided design (CAD) apparatus. The designing apparatus 21 includes the CPU 22, a memory 23, a storage device 24, a display 25, an input device 26, and a drive device 27, which are connected to one another by a bus 28.

The CPU 22 uses the memory 23 to execute a program for performing the chip size estimation of Fig. 1. The memory 23 is normally a cache memory, a system memory, a display memory, or the like. The display 25, which is used to show a processing result page or a parameter input page, is normally

a CRT, an LCD, or a PDP. The input device 26 is used by a user to input requests, instructions, and parameters, and is, for example; a keyboard and a mouse.

The storage device 24 is normally a magnetic disk device,  
5 an optical disc device, a magneto-optic disc device, or the like. The storage device 24 stores the files F1 to F9, which store programs for performing various processes and the data required to execute the programs. In response to an  
10 instruction from the input device 26, the CPU 22 transfers programs and data stored in various files to the memory 23 and sequentially executes the programs. The storage device 24 is used as a database.

Programs stored on a recording medium 29 are provided to the designing apparatus 21. The drive device 27 drives the  
15 recording medium 29 and accesses the stored contents. The CPU 22 reads programs from the recording medium 29 via the drive device 27 and installs the programs in the storage device 24.

Any type of recording medium, such as an optical disc (e.g., CD-ROM and DVD-ROM) or a magneto-optic disc (e.g., MO  
20 and MD), may be used as the recording medium 29. The recording medium 29 may also be a medium or a disk device that uploads or downloads programs via a communication medium.

The determination of the provisional quantity and provisional locations of the power supply pads (the process of  
25 step S4 in Fig. 1) will now be discussed with reference to Figs. 3 to 10.

First, in step S11 of Fig. 3, the CPU 22 performs power supply network analysis of the core section based on the power consumption file F4 and the power supply wire resistance file  
30 F8 to obtain the voltage value at each node in the core section. If each IR drop value between the nodes exceeds the maximum IR drop value, the CPU 22 suspends processing.

In step S12, the CPU 22 calculates the value of the

current flowing through each node based on the calculated voltage value at each node and the resistances between the nodes stored in the power supply wire resistance file F8.

In step S13, the CPU 22 determines the provisional  
5 quantity and provisional locations of the power supply pads based on the calculated value of the current flowing through each power supply pad and the current capacity of the associated IO buffer, which is connected to the power supply pad. More specifically, the CPU 22 compares the value of the  
10 current flowing through each power supply pad with the current capacity of the associated IO buffer. If the value of the current flowing through each power supply pad exceeds the current capacity, the CPU 22 adds a new power supply pad in the vicinity of that power supply pad. If the value of the  
15 current flowing through each power supply pad is less than or equal to the current capacity, deletion (elimination or change in type of pad) of power supply pads is enabled, as will be described later.

The processing of Fig. 3 will now be discussed in detail  
20 with reference to Fig. 4.

First, in step S20, the initialization of power supply pads is performed prior to step S11 of Fig. 3. More specifically, all of the pads (power supply pads including those at which the potential differs) arranged on the device  
25 (semiconductor integrated circuit) subject to designing are initially defined as power supply pads  $P_v$  at which the potentials are the same (Fig. 5A). Hereafter, the power supply pads  $P_v$  set at the same potential are referred to as initial power supply pads  $P_v$ .

30 Then, in step S21, the CPU 22 performs power supply network analysis based on the power consumption file F4 and the power supply wire resistance file F8 to obtain the voltage value of each node. When each IR drop value between the nodes

exceeds the maximum IR drop value, the CPU 22 suspends processing at that point in time.

In the present embodiment, the power supply network analysis is simplified by modeling the core section in the following manner. First, the interior of the core section is approximated as a plurality of power units (PUs), each of which is configured by a resistor and a power supply. The power units are electrically equivalent to one another. The voltage value at each node connecting the PUs is obtained.

10 In step S22, the CPU 22 calculates the value of the current flowing through the initial power supply pads Pv based on the resistances between the nodes (the resistances between PUs) stored in the power supply wire resistance file F8.

More specifically, referring to Fig. 6, an IO buffer Buf is connected to each power supply pad Pv arranged around the chip. Each power supply pad Pv is defined as a node N1. A node connecting the associated IO buffer Buf and the core section is defined as a node N2. When the resistance between nodes N1 and N2 is approximated with resistance R, the value Ip of the current flowing between the nodes N1 and N2 is obtained from the following equation.

$$I_p = |V_1 - V_2| / R$$

In the equation, V1 and V2 are the voltages of nodes N1 and N2. The current value Ip corresponds to the value of the current flowing through the initial power supply pads Pv.

In step S23, the CPU 22 performs an elimination process of the initial power supply pads Pv based on the calculated current value Ip and the current capacity Ic of the IO buffer Buf.

30 The elimination process will now be discussed in detail with reference to Fig. 7. From the initial power supply pads Pv, at least one pad is selected as a reference pad Ps. Among the power supply pads arranged around the chip, the CPU 22



selects a pad having a restricted location based on the pad restriction information file F9. In the preferred embodiment, a pad satisfying at least one of the conditions described below is selected as the reference pad Ps.

5       A power supply pad for which location is restricted to solve noise problems, such as simultaneous switching noise of the output buffer.

      A power supply for which location is restricted due to the specification of package pins.

10       A power supply pad having a current value that is greater than the two power supply pads arranged next to that power supply pad.

      A power supply pad at which current is concentrated (current value being greater than or equal to a predetermined value).

15       A power supply pad having a fixed location due to other restrictions of the designed device.

      Subsequent to the selection of the reference pad Ps, the CPU 22 determines whether elimination of the initial power supply pads Pv, excluding the reference pad Ps, is possible. In other words, the CPU 22 checks whether the initial power supply pads Pv may be used as pads having purposes other than those of power supply pads.

20       The elimination process is started from the two initial power supply pads Pv located next to the reference pad Ps and then performed going one-by-one to the next power supply pad Pv. More specifically, referring to Fig. 7, the current value Aa of the pad Pd subject to the elimination process is first distributed at a predetermined ratio between the reference pad Ps and an adjacent pad Pso, which is located adjacent to the pad Pd subject to the elimination process on the opposite side of the reference pad Ps.

      In this state, the distribution ratio of the current

value A is determined in accordance with the current value of each pad Ps and Pso and the distance between the subject pad Pd and each of the pad Ps and Pso. More specifically, between the two pads Ps and Pso, more current is distributed to the pad having a greater current value and to the pad that is closer to the subject pad Pd. When Ab represents the current value of the reference pad Ps, Ac represents the current value of the pad Pso, L1 represents the distance between the subject pad Pd and the pad Pso, and L2 represents the distance between the subject pad Pd and the reference pad Ps, the distributed amounts X1 and X2 of the current value A to the pads Pso and Ps are determined from the next equation.

Equation 1

$$X1 = \frac{Aa \{ Ac / (Ab + Ac) + L2 / (L1 + L2) \}}{2}$$

$$X2 = \frac{Aa \{ Ab / (Ab + Ac) + L1 / (L1 + L2) \}}{2}$$

It is presumed that the changing rate of the current amount corresponding to movement of a predetermined unit distance is constant regardless of the location of the subject pad Pd.

As a result, the current value of the reference pad Ps subsequent to the current distribution is represented by (Ab+X2). In the present embodiment, the current value (Ab+X2) of the reference pad Ps subsequent to current distribution is compared with the current capacity Ic of the IO buffer Buf connected to the reference pad Ps to determine whether elimination of the subject pad Pd is possible.

If the current value (Ab+X2) does not exceed the current capacity Ic ( $Ic \geq (Ab+X2)$ ), the CPU 22 returns (assigns) the subject pad Pd to a state prior to the initialization process (signal pad or power supply pad having a different potential)

of step S20. If the current value ( $Ab+X2$ ) exceeds the current capacity  $Ic$  ( $Ic < (Ab+X2)$ ), the CPU 22 uses the subject pad  $Pd$  as a power supply pad and determines the location of the subject pad  $Pd$ .

5        Afterwards, in the same manner, the CPU 22 sequentially performs the elimination process on all of the initial power supply pads  $Pv$  excluding the reference pad  $Ps$ . Referring to Fig. 5(b), the reference pad  $Ps$  and the pads that were not eliminated during the elimination process are provisionally  
10        determined as the power supply pads.

      In step S24, the CPU 22 determines whether completion conditions are satisfied. The completion conditions include whether or not pads have been eliminated in the previous elimination process. When there are no eliminated pads, the  
15        CPU 22 determines that there is no necessity to further perform the elimination process and ends the process of Fig. 4.

      When there is an eliminated pad, the CPU 22 determines that the elimination process has not been completed and  
20        returns to step S21 to perform the power supply network analysis again. Then, the CPU 22 repeats the current amount calculation of step S22 and the elimination process of step S23. When performing the elimination process for a second time, from the initial power supply pads  $Pv$  that were not  
25        selected in the first elimination process, the CPU 22 selects the pad having the greatest current value as the reference pad  $Ps$ . Steps S21 to S23 are repeated until the CPU 22 determines that the elimination process has been completed in step S24.

      When the quantity of power supply pads is restricted due  
30        to the specification of package pins or the like, the locations of the power supply are changed as described below to optimize the routing of the power supply pads.

      After determining the provisional quantity and

provisional locations of the power supply pads, the CPU 22 compares the current value of the power supply pad of which location is to be changed with the current value of an adjacent power supply (signal pads between the power supply pads are ignored). The CPU 22 moves power supply pads having small current values toward power supply pads having large current values. When the distance between the two power supply pads is represented by L, and the current values of the two power supply pads are represented by Ia and Ib ( $I_a > I_b$ ), the movement amount D is determined through the following equation.

Equation 2

$$D = L((I_a - I_b) / I_a)$$

In the present embodiment, the items described below are taken into consideration so that the provisional quantity and provisional locations of the power supply pads are accurately determined prior to the layout of the circuitry and to optimize the quantity and locations of the power supply pads during the layout of the circuitry and after the layout of the circuitry.

[1. Bias of power supply wire density in the core section]

When routing power supply wires in the core section C, for example, referring to Fig. 8, the arrangement of macros M1 and M2 would result in the necessity of breaking power supply wires (three are broken in Fig. 8) or detouring the macros M1 and M2. This would bias the power supply wire density in the core section C. Such bias of the power supply wire density is extracted from the layout data. Information related to the bias is stored in the power supply wire resistance file F8. The CPU 22 refers to the power supply wire resistance file F8 to perform power supply network analysis in order to optimize the quantity and locations of the power supply pads while taking into consideration the bias of the power supply wire

density.

[2. Bias of power consumption in the core section]

Referring to Fig. 9, when the core section C includes modules M3 and M4, which operate at relatively high speeds, the power consumption of the core section C is biased in accordance with the locations of the modules M3 and M4.

Information related to the bias of the power consumption is stored in the power consumption file F4 for each designed inductance or each module. The CPU 22 refers to the power consumption file F4 when performing power supply network analysis so that the provisional quantity and provisional locations of the power supply pads are determined with high accuracy while taking into consideration the bias of the power consumption.

[3. Bias of current amount in power supply pad]

The amount of current flowing through the power supply pad differs depending on the location of the power supply pad. Referring to Fig. 10, in each side of a chip, the current amount normally increases as the center becomes closer and decreases as the ends become closer. Further, when power supply pads are located adjacent to power supply pads supplying power having different potentials, current tends to concentrate at those power supply pads. Such bias of the current amount is calculated beforehand to take into consideration bias of the current amount when performing power supply analysis. This enables the provisional quantity and provisional locations of the power supply pads to be determined with high accuracy.

The process for estimating the core size in step S3 of Fig. 1 will now be discussed.

Fig. 11 is a flowchart illustrating the process for estimating the core size.

Prior to estimation of the core size, the circuit

information file F6 and the layout parameter file F7 are prepared. Parameters related to various circuit information extracted from the netlist file F1 (e.g., cell quantity  $N_{cell}$ , total net quantity  $J$ , average fan-out  $m_{avg}$ , average cell area  $A_{cell}$ , and total area of the used macro (total macro area)  $A_{macro}$ ) are recorded in the circuit information file F6. Parameters related to layout design (e.g., cell usage rate  $p$ , wire layer quantity  $K$ , coefficient corresponding to aspect ratio (length and width ratio) of a circuit block  $z_A$ ) are stored in the layout parameter file F7. The cell usage rate is a value obtained by dividing the total cell area in the core section by the area of the region enabling the arrangement of cells in the core section.

In step S31a, the total net length of the core section is calculated based on the circuit information file F6 and the layout parameter file F7. At the same time, in step S31b, the usable channel length is calculated based on the circuit information file F6 and the layout parameter file F7.

The calculation of the total net length in step S31a will now be discussed. Step S31a includes calculation of the average path length (step S311a) and calculation of the total net length (step S312a).

[Step S311a, calculation of average path length]

In step S311a, the average path length of each net in the core section is calculated. The path length is the length of a wire from an input terminal to an output terminal. The average path length  $L_{path-idf.avg}$  is obtained from the next equation using the cell quantity  $N_{cell}$ , the average cell area  $A_{cell}$ , the cell usage rate  $p$ , and the Rent's exponent  $p$ .

Equation 3

$$L_{\text{path-idf,avg}} = \frac{\frac{p-0.5}{p} - \sqrt{N_{\text{cell}}} - \frac{p-0.5}{6\sqrt{N_{\text{cell}}}(p+0.5)} + N_{\text{cell}}^p \frac{4^{p-0.5} - p - 1}{2(p+0.5)p(p-1)}}{N_{\text{cell}}^{p-0.5} \frac{2^{2p-1} - 2p - 1}{2p(p-1)(2p-3)} - \frac{p-0.5}{6p\sqrt{N_{\text{cell}}}} + 1 - \frac{\sqrt{N_{\text{cell}}}(p-0.5)}{p-1}} \times \sqrt{\frac{A_{\text{cell}}}{p}}$$

(refer to J.A. Davis, V.K. De, J.D. Meindl "A Stochastic Wire-  
Length Distribution for Gigascale Integration (GSI)- Part II :  
Applications to Clock Frequency, Power Dissipation, and Chip  
Size Estimation", IEEE Transaction on Electron Devices,  
Vol.45, No.3, March 1998)

The average path length  $L_{\text{path-idf,avg}}$  is obtained as a  
Manhattan length (minimum distance connecting two ends with a  
combination of horizontal and vertical lines). The Rent's  
exponent  $p$  is calculated from the following equation using the  
cell quantity  $N_{\text{cell}}$ , the total net quantity  $J$ , and the average  
fan-out  $m_{\text{avg}}$ , which are dependent on the circuit architecture.  
Equation 4

$$p = \log_{N_{\text{cell}}} \left( 1 - \frac{(m_{\text{avg}} + 1) \cdot J}{a \cdot J \cdot m_{\text{avg}} + b \cdot N_{\text{cell}}} \right) + 1$$

In the equation, the coefficients  $a$  and  $b$  are values  
obtained from layout information obtained through past  
experience. In the circuit information, when some parameters  
are not determined (average fan-out  $m_{\text{avg}}$  etc.), a predetermined  
default value may be used as the Rent's exponent  $p$ . In the  
equation for calculating the Rent's exponent  $p$ , the gate  
quantity may be used in lieu of the cell quantity  $N_{\text{cell}}$ . In  
such a case, the gate quantity may be the average gate  
quantity per cell that is calculated beforehand.

[Step S312a, calculation of total net length]

In step S312a, the total length of all of the wires  
configuring the core section (total net length) is calculated

based on the fan-out of each net.

Among all of the nets, when the total of the nets having a fan-out of  $m$  is represented by  $J_{FO=m}$ , the net length  $L_{net.FO=m}$  of the nets having fan-out  $m$  is obtained from the following

5 equation using the average path length  $L_{path-idf.avg}$ .  
Equation 5

$$L_{net.FO=m} = L_{path-idf.avg} \times t(m) \times J_{FO=m}$$

In the equation,  $t(m)$  is a function correlated with the fan-out  $m$  and the influence of detouring wires in the net of  
10 the fan-out  $m$ .

Equation 6

$$t(m) = m \times a_{FO=m} \times b_{FO=m}$$

In the equation,  $a_{FO=m}$  is a function for obtaining the average path length of the net of the fan-out  $m$ . Further,  $b_{FO=m}$   
15 is a function for converting the average path length of the net of the fan-out  $m$  to average net length. Accordingly, in equation 5,  $L_{path-idf.avg} \times t(m)$  is represented as the average net length  $L_{net-avg.FO=m}$  of the fan-out  $m$ . Each of the functions  $a_{FO=m}$  and  $b_{FO=m}$  is expressed using the fan-out  $m$ .

20 Equation 5 is used to calculate the net length of each net in accordance with the fan-out. The total of the net lengths of the fan-out is obtained as the total net length  $L_{net-total}$  forming the core section. In other words, the total net length  $L_{net-total}$  is expressed from the following equation.

25 Equation 7

$$L_{net-total} = \sum L_{net.FO=m}$$

In accordance with the next equation, the total length (net length  $L_{net-total.x}$ ) of a wire (first wire) in a first direction (e.g., the X axis direction in Fig. 14) and the  
30 total length (net length  $L_{net-total.y}$ ) of a wire (second wire) in



a second direction (e.g., the Y axis direction in Fig. 14), which is perpendicular to the first direction along a horizontal plane, is obtained from the total net length  $L_{\text{net-total}}$ .

$$L_{\text{net-total}, X} = L_{\text{net-total}} \times Z_A$$

$$L_{\text{net-total}, Y} = L_{\text{net-total}} \times (1 - Z_A)$$

5

In the equation,  $z_A$  represents the aspect ratio ( $0 < Z_A < 1$ ).

Then, the calculation of the usable channel length in step 31b will now be described. Step 31b includes estimation of the area of the core section (step S311b) and calculation of the usable channel length (step S312b).

10

[Step S311b, estimation of area of core section]

In step 311b, the cell quantity  $N_{\text{cell}}$ , the average cell area  $A_{\text{cell}}$ , the cell usage rate  $\rho$ , and the total macro area  $A_{\text{macro}}$  are used to estimate the core section area  $A_{\text{temp-area}}$ . The estimated core section area  $A_{\text{temp-area}}$  is the sum of the total area of the cells arranged in the core section and the total macro area  $A_{\text{macro}}$ .

15

Equation 9

$$A_{\text{temp-area}} = (A_{\text{cell}} / \rho) \times N_{\text{cell}} + A_{\text{macro}}$$

20

[Step S312b, calculation of usable channel length]

In step S312b, the usable channel length in each wire layer is calculated based on the estimated core section area  $A_{\text{temp-area}}$ .

25

In the following equation, the usage channel length  $L_{\text{usable}, n}$  of a certain wire layer  $n$  is the ideal usable channel length  $L_{\text{all}, n}$  when presuming that the whole surface of the wire layer  $n$  is a routable region. The routing prohibition length of the wire layer  $n$  is represented by  $L_{\text{prohibit}, n}$ . The maximum channel usage rate of the wire layer  $n$  is represented by  $r_n$ .

Equation 10

$$L_{usable, n} = (L_{all, n} - L_{prohibit, n}) \times r_n$$

The ideal usable channel length  $L_{all, n}$  in the wire layer  $n$  is obtained from the value of the estimated area  $A_{temp-area}$  and the aspect ratio  $Z_A$ . The wire prohibition channel length  $L_{prohibit, n}$  is obtained by adding the channel length used for power supply wires, the channel length that is lost by the arrangement of a hard macro, the channel length of when a wire channel is substantially lost in an intermediate wire layer due to a stuck via hole produced when an upper wire layer is connected to a lower wire layer, and the channel length is known to be unusable from the beginning.

In the same manner, equation 10 is used to calculate the usable channel length in other wire layers. Then, the usable channel length of all of the wire layers is added to obtain the usable channel length  $L_{usable-total}$  of all of the wire layers. The usable channel length  $L_{usable-total}$  of all of the wire layers is obtained from the next equation.

Equation 11

$$L_{usable-total} = \sum L_{usable, n}$$

20

The routing direction is normally determined for each wire layer. The usable channel length  $L_{usable-total, x}$  for wires routed in the first direction along a horizontal plane and the usable channel length  $L_{usable-total, y}$  for wires routed in the second direction, which is perpendicular to the first direction, along the horizontal plane are each obtained by adding the usable channel lengths of wire layers having the same routing direction. The usable channel length  $L_{usable-total, x}$  of the first direction is obtained by adding usable channel

lengths of wire layers on which wires are routed in the first direction. The usable channel length  $L_{usable-total.Y}$  of the second direction is obtained by adding usable channel lengths of wire layers on which wires are routed in the second direction.

5 In step S32, the total net lengths  $L_{net-total}$ ,  $L_{net-total.X}$ , and  $L_{net-total.Y}$  obtained in step S31a are respectively compared with the usable channel lengths  $L_{usable-total}$ ,  $L_{usable-total.X}$ , and  $L_{usable-total.Y}$  to determine whether all of the following conditions are satisfied.

10 Equation 12

$$L_{net-total} \leq L_{usable-total}$$

$$L_{net-total.X} \leq L_{usable-total.X}$$

$$L_{net-total.Y} \leq L_{usable-total.Y}$$

When all of the conditions are satisfied, the routing of wires in the estimated area  $A_{temp-area}$  is enabled. Accordingly, the value of the estimated area  $A_{temp-area}$  is determined as the  
15 core size (step S33). When any one of the conditions is not satisfied, the layout parameter is changed and processing is restarted from step S311b. In this case, the cell usage rate  $\rho$  is decreased or the wire layer quantity  $K$  is increased to increase the estimated area to the minimal area that satisfies  
20 the conditions of equation 12.

The core size decreases as the cell usage rate  $\rho$  increases. The core size (estimated area  $A_{temp-area}$ ) becomes minimal when the cell usage rate  $\rho$  is 100%. In other words, in such a state, the core section is fully routed without any  
25 gaps. However, routing is seldom enabled in a state in which the cell usage rate  $\rho$  is 100%. The maximum value of the cell usage rate  $\rho$  is normally less than 100% depending on the layout tool, the density of wires, and the layout TAT. The estimated area  $A_{temp-area}$  of the core section is efficiently

calculated by setting the maximum value of the cell usage rate  $p$  in accordance with such a designing environment.

In the preferred embodiment, the total net length  $L_{\text{net-total}}$  is calculated taking into consideration the fan-out of each net. Further, the core size is estimated based on the total net length  $L_{\text{net-total}}$ . As a result, the core size is estimated while accurately estimating the total wire length of the wires routed on the core section. Thus, the provisional wire capacitance value of each net may also be accurately estimated in accordance with the fan-out of each net and the estimated area of the core section in the present embodiment.

For example, the provisional wire capacitance value of a net of the fan-out is obtained from the product of the average net length  $L_{\text{net-avg.FO=m}}$  of the fan-out  $m$  and the wire capacitance value. The average net length  $L_{\text{net-avg.FO=m}}$  of the fan-out  $m$  is obtained from " $L_{\text{path-idf.avg}} \times t(m)$ " (refer to equation 5). Further, the average net length  $L_{\text{net-avg.FO=m}}$  is a value proportional to the cell quantity  $N_{\text{cell}}$  included in the core section. Accordingly, the provisional wire capacitance value of the net of the fan-out is accurately estimated in accordance with the fan-out  $m$  and the core size of each net.

The first embodiment has the advantages described below.

(1) The value of the current that flows through a power supply pad is calculated from the voltage value of each node that is obtained through the power supply network analysis. The current value and the current capacity of the IO buffer is then compared to determine the provisional quantity and provisional locations of the power supply pads. The provisional quantity and provisional locations of the power supply pads that guarantee the SI and PI taking into consideration the current capacity of the IO buffer are accurately estimated prior to the detailed layout. This decreases redesigning, shortens the design time, and reduces

design costs.

(2) After the power supply network analysis, processing is suspended when the IR drop value between nodes exceeds the maximum IR drop value. Accordingly, the provisional quantity and the provisional locations of the power supply pads that satisfy the IR drop conditions in the core section are used for the detailed layout of circuitry.

(3) In the present embodiment, the power supply network analysis is performed by modeling a core section as a plurality of equivalent circuits (PU) that are electrically equivalent to one another in the core section. The determination of the provisional quantity and provisional locations of the power pads is facilitated by simplifying the power supply network analysis. Further, the power supply network analysis time is shortened and the design time is shortened.

(4) In the present embodiment, a power supply pad of which location is restricted is used as the reference pad Ps. Further, the elimination process is performed on power supply pads (initial power supply pads Pv) excluding the reference pad Ps. This accurately determines the provisional quantity and provisional locations of the power supply pads while taking into consideration such routing restrictions.

(5) In the present embodiment, the power supply network analysis is performed taking into consideration the bias of power consumption in the core section to accurately determine the provisional quantity and provisional locations of the power supply pads.

(6) In the present embodiment, the power supply network analysis is performed taking into consideration the bias of the amount of current flowing through the power supply pads to accurately determine the provisional quantity and provisional locations of the power supply pads.

(7) In the present embodiment, the power supply network analysis is performed taking into consideration the bias of the power supply wire density in the core section to optimize the quantity and locations of the power supply pads subsequent  
5 to layout.

(8) The core size is estimated from the result obtained by calculating the total net length  $L_{\text{net-total}}$  from the average path length  $L_{\text{path-idf.avg}}$  taking into consideration the fan-out of each net and then comparing the total net length  $L_{\text{net-total}}$  with  
10 the usable channel length  $L_{\text{usable-total}}$ . The core size is estimated taking into consideration the fan-out of each net. Thus, the core size is estimated accurately at a minimal area without actually performing a layout.

(9) In the present embodiment, when the total net length  
15  $L_{\text{net-total}}$  and the usable channel length  $L_{\text{usable-total}}$  is compared, components of the wiring direction in the first and second directions are also compared. This estimates the core size further accurately.

(10) In the present embodiment, the quantity and  
20 locations of the power supply pads and the core size are accurately estimated. This enables the chip size to be accurately estimated prior to layout.

(11) In the core size estimation of the present embodiment, the average net length  $L_{\text{net-avg.FO=m}}$  is accurately  
25 obtained in accordance with the fan-out of each net. Thus, the provisional wire capacitance value of each net is accurately estimated. Accordingly, the performance of an LSI may be evaluated with high accuracy prior to layout of the circuitry.

A designing method and a designing apparatus of a  
30 semiconductor integrated circuit according to a second embodiment of the present invention will now be discussed centering on parts differing from the first embodiment. The second embodiment differs from the first embodiment in the

core size estimation process of step S13 in Fig. 1. In the second embodiment, the size of a core section configured by a plurality of circuit blocks is estimated.

5 In step S41 of Fig. 12, the area of each circuit block configured in the core section and the total area of all of the circuit blocks are calculated. The area of a circuit that has been laid out in the past does not have to be calculated again. Thus, the area obtained in the past layout is used. For a circuit block that is laid out for the first time, the  
10 area may be estimated through the core size estimation of the first embodiment.

In step S42, the total area of the wire region required to route wires around each circuit block and the total area of all of such wire regions is calculated. For example, referring  
15 to Fig. 13, a circuit block 32 and a wire region 33, which extends around the circuit block 32, is regarded as a layout surface (layout block in Fig. 13) to obtain the total bottom surface area of all of such layout blocks 31. Step S42 will be described in detail later.

20 In step S43, the total area of repeater cells arranged between the circuit blocks 32 is calculated. When a wire connecting circuit blocks to each other is long, a repeater cell, which functions as a buffer circuit, is arranged in the wire to decrease path delay. Step S43 will be described in  
25 detail later.

In step S44, the sum of the total area of all of the layout blocks (i.e., the total area of all of the wire regions 33 and the total area of all of the circuit blocks 32) and the total area of the repeater cells are calculated to estimate  
30 the core size.

Step S42 (calculation of the area of wire region 33) will now be discussed with reference to Figs. 14 to 16. Fig. 14 is a plan view of the circuit block 32. For the sake of brevity,

the direction parallel to the X axis is referred to as a first direction, and the direction parallel to the Y axis is referred to as a second direction. As viewed in Fig. 14, the right side and left side of the circuit block 32 are parallel to the Y axis. The upper side and lower side of the circuit block 32 are parallel to the X axis. The procedures for obtaining the wire region required for routing wires outside the left and right sides of the circuit block 32 will now be discussed. The wire regions outside the upper and lower sides of the circuit block 32 are obtained in the same manner.

[Process 1]

The quantity of wires required for routing terminals for the circuit block 32 is calculated.

As shown in Fig. 14, the wire quantities  $I_L$  and  $I_R$ , which are the quantities of the wires respectively extending from the left and right sides of the circuit block 32, are respectively equal to the terminal quantities  $T_L$  and  $T_R$ , which are the quantity of terminals extending from the left and right sides of the circuit block 32. Wire Quantity  $I_L$  = Terminal Quantity  $T_L$  (left side), Wire Quantity  $I_R$  = Terminal Quantity  $T_R$  (right side)

[Process 2]

The quantity  $I_{\text{detour}}$  of wires that detour the circuit block 32 to connect other circuit blocks 32 is calculated.

When the circuit block 32 lies between other circuit blocks, wires connecting the circuit blocks passes by the layout block 31. Wires passing by the layout block 31 include wires passing over the circuit block 32 and wires (detouring wires) passing over the wire region 33 outside the circuit block 32. In process 2, the quantity  $I_{\text{detour}}$  of the detouring wires are obtained.

Fig. 16 is a flowchart illustrating a procedure for calculating the wire quantity  $I_{\text{detour}}$ .



In step S51, the wire quantity  $I_{thru}$  that passes by the layout block 31 is estimated. When the quantity of circuit blocks included in a core section is represented by  $N_{block}$ , the total net quantity between circuit blocks is represented by  $J_B$ , the average fan-out is represented by  $m_{avg}$ , the Rent's exponent is represented by  $p$ , and the ratio of wires passing by the layout block 31 among the wires that are not used to connect adjacent circuit blocks is represented by  $c$  ( $0 \leq c \leq 1$ ), the estimated wire quantity  $I_{thru}$  is calculated from the next equation.

Equation 13

$$I_{thru} = J_B \times m_{avg} \times \left[ 1 - \frac{\frac{2^{2p}-1}{6p} - \frac{2\sqrt{N_{block}}(2^{2p-1}-1)}{2^{2p-1}} + \frac{N_{block}(2^{2p-2}-1)}{p-1}}{\frac{N_{block}^p(2^{2p-1}-2^{2p-1})}{p(2p-1)(p-1)(2p-3)} - \frac{1}{6p} + \frac{2\sqrt{N_{block}}}{2^{2p-1}} - \frac{N_{block}}{p-1}} \right] \times c$$

In step S52, it is determined whether or not the wires passing by the layout block 31 pass over the circuit block 32. In other words, it is determined whether wires can be routed over the circuit block 32. More specifically, the routing channel quantity  $I_{ch.usable}$ , which is the quantity of channels that are routable over the circuit block 32 is obtained. When the routing channel quantity  $I_{ch.usable}$  is zero, it is determined that routing over the circuit block 32 is not possible. The routing channel quantity  $I_{ch.usable}$  does not include channels that are not routable due to power supply wires.

When routing over the circuit block 32 is not possible (NO in step S52), the wires that pass by the layout block 31 all detour the circuit block 32. In other words, the relationship of  $I_{detour} = I_{thru}$  is satisfied. Fig. 15 is a schematic diagram showing a state in which when the

relationship of  $I_{\text{detour}} = I_{\text{thru}}$  is satisfied, among the wires that pass by the layout block 31,  $I_{\text{thru}}/2$  passes by each of the left and right sides of the circuit block 32.

When routing of the circuit block 32 is possible (YES in step S52), the process proceeds to step S53. In step S53, the interval  $d_r$  of repeater cells arranged in wires connecting circuit blocks is compared with the length  $L_{\text{block}}$  of the sides of the circuit block 32 extending in a direction that is parallel to the wires including the repeater cells (the direction of the Y axis in Fig. 15).

Under the condition of  $d_r < L_{\text{block}}$  (NO in step S53), routing for connecting circuit blocks cannot be performed over the circuit block 32. Thus, in the same manner as described above, the wires that pass by the layout block 31 all detour the circuit block 32 (i.e.,  $I_{\text{detour}} = I_{\text{thru}}$ ).

Under the condition of  $d_r > L_{\text{block}}$  (YES in step S53), routing for connecting circuit blocks can be performed over the circuit block 32 via repeater cells. In this case, the process proceeds to step S54 to compare the wire quantity  $I_{\text{thru}}$  that passes by the layout block 31 with the routing channel quantity  $I_{\text{ch.usable}}$  of the circuit block 32 and determine whether the routing channel quantity  $I_{\text{ch.usable}}$  is greater than the wire quantity  $I_{\text{thru}}$ .

Under the condition of  $I_{\text{thru}} < I_{\text{ch.usable}}$  (YES in step S54), the wires that pass by the layout block 31 are all wires that pass over circuit block 32. In other words, the relationship of  $I_{\text{detour}} = 0$  is satisfied.

Under the condition of  $I_{\text{thru}} > I_{\text{ch.usable}}$  (NO in step S54), the difference between the wire quantity  $I_{\text{thru}}$  and the routing channel quantity  $I_{\text{ch.usable}}$  is the quantity of wires that pass over the circuit block 32. In this case, the relationship of  $I_{\text{detour}} = I_{\text{thru}} - I_{\text{ch.usable}}$  is satisfied.

[Process 3]

The sum of the wire quantities  $I_L$  and  $I_R$  obtained in process 1 and the wire quantity  $I_{\text{detour}}$  obtained in process 2 is calculated. The sum  $I_{oh}$  of the wire quantities is the

5 estimated value of the total quantity of wires that pass by the outer side of the circuit block 32 (in this case, the left and right outer sides of the circuit block 32).

Equation 14

10 
$$I_{oh} = I_L + I_R + I_{\text{detour}}$$

[Process 4]

The minimal wire region area that satisfies the wire quantity sum  $I_{oh}$  obtained in process 3 is obtained.

15 The minimal wire region area is determined so that the product of the wire interval in each wire layer (e.g., wire interval in the direction of the Y axis) and routing channel quantity is the same in every wire layer and so that the sum of the routing channel quantity in every wire layer is the  
20 same as the sum  $I_{oh}$ . The usable routing channel quantity in each wire layer increases as the quantity of wire layers increases. This decreases the wire region. Like the routing channel quantity of the circuit block 32 described above, the routing channel quantity does not includes channels that  
25 cannot be routed due to power supply wires.

The area of the wire region that is to be provided on the outer left and right sides of the circuit block 32 is obtained by performing processes 1 to 4. The area of the wire region that is to be provided on the outer upper and lower sides of  
30 the circuit block 32 is also obtained by performing processes 1 to 4.

When the length of the upper and lower sides of the circuit block 32 is represented by  $L_{\text{block},x}$ , the length of the

left and right sides of the circuit block 32 is represented by  $L_{\text{block},Y}$ , and the length of the wire region required for the upper, lower, left, and right sides of the layout block 31 obtained through processes 1 to 4 are respectively represented  
 5 by  $L_T$ ,  $L_B$ ,  $L_L$ , and  $L_R$ , the area  $A_{\text{block-add}}$  of the circuit block 32 to which the wire region 33 is added (i.e., layout block 31) is calculated with the next equation.  
 Equation 15

$$A_{\text{block-add}} = (L_{\text{block},X} + L_L + L_R) \times (L_{\text{block},Y} + L_T + L_B)$$

10 Accordingly, the total value  $A_{\text{block-add-all}}$  of the area of the layout block including the required wire regions for all of the circuit blocks configured on the core section is represented by the next equation.  
 Equation 16

$$A_{\text{block-add-all}} = \sum A_{\text{block-add}}$$

15

The procedure for calculating the area (total value) of the repeater cells used to connect circuit blocks will now be discussed.

The total value of the repeater cell area is obtained  
 20 from the product of the quantity  $N_{\text{buffer}}$  of the repeater cells configured in the core section and the estimated area  $A_{\text{buffer}}$  of each repeater cell.

The repeater cell quantity  $N_{\text{buffer}}$  of the core section is calculated from the following equation.

Equation 17

$$N_{buffer} = 0 \times \int_1^{l_r} i(l) dl + 1 \times \int_{l_r}^{2l_r} i(l) dl + 2 \times \int_{2l_r}^{3l_r} i(l) dl + \dots + z \times \int_{zl_r}^{2\sqrt{N}} i(l) dl$$

$$i(l) = \frac{\alpha k}{2} \Gamma \left( \frac{l^3}{3} - 2\sqrt{N_{block}} l^2 + 2Nl \right) l^{2p-4} \quad \left( 1 \leq l \leq \sqrt{N_{block}} \right)$$

$$i(l) = \frac{\alpha k}{6} \Gamma \left( 2\sqrt{N_{block}} - l \right)^3 l^{2p-4} \quad \left( \sqrt{N_{block}} \leq l \leq 2\sqrt{N_{block}} \right)$$

$$k = \frac{(m_{avg} + 1) J}{N_{block} (1 - N_{block}^{p-1})}$$

$z$  is the maximum integer satisfying  $z \cdot l_r < 2\sqrt{N_{block}}$

- 5 The gate pitch, which is represented by  $l_r$ , is calculated from the following equation and obtained from the average layout block area  $A_{block-add-avg}$ , which is calculated from the total value  $A_{block-add-all}$  of the area of the layout block.

Equation 18

$$l_r = (A_{block-add-avg})^{0.5} / d_r$$

10

Accordingly, the total area  $A_{buffer-total}$  of the repeater cell is calculated from the following equation.

Equation 19

$$A_{buffer-total} = A_{buffer} \times N_{buffer}$$

- 15 Therefore, the estimated area  $A_{core}$  of the core section is obtained from the sum of the total value  $A_{block-add-all}$  of the layout block area and the total value  $A_{buffer-total}$  of the repeater cell area through the following equation.

Equation 20

$$A_{core} = A_{block-add-all} + A_{buffer-total}$$

20

The estimation of the core size in the present embodiment enables the minimum area (core size) of the core section

configured by a plurality of circuit blocks to be accurately estimated.

The second embodiment has the advantages described below.

(1) When the core section is configured by a plurality of circuit blocks, the core size is estimated as being the total area of the area of each circuit block, the wire region required when connecting circuit blocks, and the area of repeater cells that connect circuit blocks. This enables the minimum area of the core section, which is configured by a plurality of circuit blocks, to be accurately estimated.

It should be apparent to those skilled in the art that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Particularly, it should be understood that the present invention may be embodied in the following forms.

In the procedure of the first embodiment that determines the provisional quantity and provisional locations of the power supply pads (Fig. 4), processing may be started in a state in which one power supply pad is provided for each side of a chip (the potential at each pad being the same). Then, power supply pads are added in accordance with the comparison between the value of the current flowing through each pad and the current capacity of the IO buffer.

In the first embodiment, the criterion for selecting the reference pad  $P_s$  may be changed.

In addition to a core section having a plurality of circuit blocks, the core size estimation of the second embodiment may be performed on a core section having only one circuit block.

The present examples and embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalence of the appended claims.